UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

KAIST IP US LLC,

Plaintiff and Counterclaim-Defendant,

v.

SAMSUNG ELECTRONICS CO., LTD.;
SAMSUNG ELECTRONICS AMERICA, INC.;
SAMSUNG SEMICONDUCTOR, INC.;
SAMSUNG AUSTIN SEMICONDUCTOR, LLC;
GLOBALFOUNDRIES, INC.;
GLOBALFOUNDRIES U.S. INC.; and
QUALCOMM INC.,

Defendants and Counterclaim-Plaintiffs.

Case No.: 2:16-cv-01314-JRG-RSP

JURY TRIAL DEMANDED

Honorable Rodney Gilstrap

FILED UNDER SEAL

MOTION BY KAIST IP US FOR SUMMARY JUDGMENT OF INFRINGEMENT AGAINST THE SAMSUNG DEFENDANTS

TABLE OF CONTENTS

TABLE OF AUTHORITIES

Federal Cases

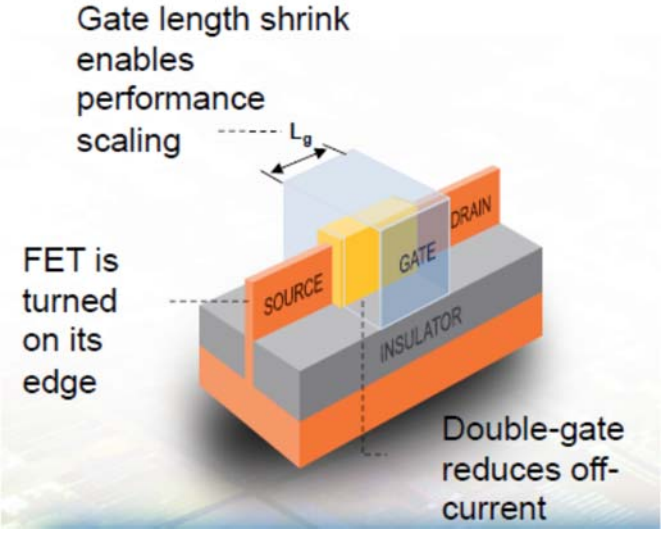
Federal Rules

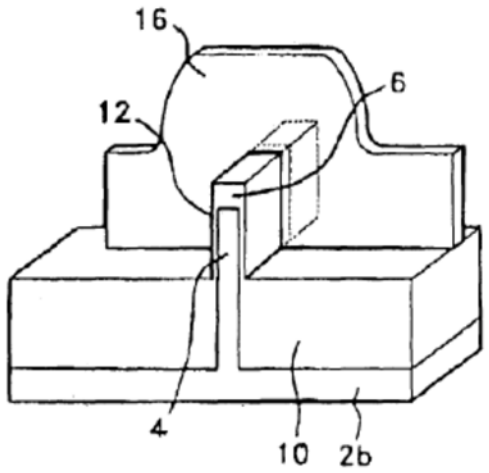
KIPB LLC, formerly known as KAIST IP US LLC ("KAIST IP US"), hereby moves for summary judgment of infringement of U.S. Patent No. 6,885,055 ("'055 Patent") by the accused bulk FinFET devices, chips, and products of Defendants Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor, LLC (collectively, "Samsung").

I. INTRODUCTION

The '055 Patent is directed to bulk "FinFET" devices, a type of field-effective transistor ("FET"). At a time when the vast majority of industry players, including the defendants in this lawsuit, had discounted bulk FinFET devices and were focused almost exclusively on silicon-on-insulator ("SOI") approach for FinFET, the '055 Patent inventor, Professor Jong-Ho Lee defied both convention and tradition to develop the first commercially viable, bulk FinFET device for application chips. This is what is embodied in the '055 Patent's claims at issue in this motion.

Below is Samsung's own depiction of the accused products, and one of the figures from the '055 Patent.





Dkt. 113-2 (KAIST-019397) (left) (illustrating a conceptual representation of Samsung's double-

gate FinFET device); Declaration of Guy Rodgers,[1] Ex. 1 ('055 Patent, Fig. 3a) (right).

The similarities between the respective parties' devices are not accidental. In fact, Professor Lee has had extensive interactions with Samsung and its engineers, whose technology is at issue in this case, dating back to the early 2000s. And it is through these interactions that Samsung was informed of the technical details of Professor Lee's invention.

For example, in or around the 2001 time-frame, Professor Lee provided guidance and training to one of Samsung's graduate students at Seoul National University about his bulk FinFET invention, which included efforts to fabricate a working FinFET. Through 2003, Samsung and a number of its engineers (including the aforementioned graduate student) used Professor Lee's designs to produce its own FinFETs. Samsung invited Professor Lee to provide numerous lectures to its engineers about Professor Lee's bulk FinFET invention.

Despite this long-standing history between Samsung and Prof. Lee, Samsung now claims that its accused devices are significantly different from the '055 Patent invention, and do not infringe the claims of the '055 Patent. But a limitation-by-limitation analysis quickly reveals that Samsung's accused products do in fact practice the claims of the '055 Patent. For the reasons set forth below, KAIST IP US respectfully requests that the Court grant summary judgment that Samsung infringes the '055 Patent.

II. STATEMENT OF ISSUES TO BE DECIDED BY THE COURT

(1.) Whether the Court should grant summary judgment of infringement as to Claims 1, 3, 4, 6, 11-13, and 15 of the '055 Patent against Samsung.

[1] "Ex." refers to exhibits to the Declaration of Guy Rodgers filed in support of this motion.

III. STATEMENT OF UNDISPUTED MATERIAL FACTS

A. The Parties

KAIST IP US is the international branch of KIP Co. Ltd., formerly known as KAIST IP Co., Ltd. ("KAIST IP"). KAIST IP was formed by the Korea Advanced Institute of Science and Technology ("KAIST") and Patent & Information Business Co., Ltd. ("P&IB") to promote the innovation and intellectual property of research-oriented science and engineering institutions in South Korea. KAIST IP US is the owner by assignment of all rights in the '055 Patent.

Samsung is one of the world's largest sellers of mobile communications devices, such as smartphones, tablets, and smart watches. Relevant to this lawsuit, Samsung manufactures systems-on-chips ("SOCs"), including its Exynos line and Qualcomm's Snapdragon line, utilizing 14 nanometer (nm) bulk FinFET process technology.

B. The '055 Patent

The '055 Patent invention covers a specific bulk FinFET design and structure. This Motion relates to asserted independent claim 1 and its dependent claims 3, 4, 6, 11-12, and 15, as well as independent claim 13.

Independent claim 1 of the '055 Patent recites:

> A double-gate FinFET device, comprising:
> (a) a bulk silicon substrate;
> (b) a Fin active region which is a wall-shape single crystalline silicon on a surface of the bulk silicon substrate and connected to said bulk silicon substrate;
> (c) a second oxide layer which is formed up to a certain height of the Fin active region from the surface of bulk silicon substrate;
> (d) a gate oxide layer which is formed on both side-walls of the Fin active region protruded from said second oxide layer;
> (e) a first oxide layer which is formed on the upper surface of said Fin active region with a thickness greater or equal to that of the gate oxide;
> (f) a gate which is formed on said first and second oxide layer;
> (g) a source/drain region which is formed on both sides of the Fin active region except where said gate overlaps with the Fin active region; and
> (h) a contact region and a metal layer which are formed at said source/drain and gate contact region,

(i) wherein the thickness of said gate oxide layer is between 0.5 nm and 10 nm, and the thickness of said first oxidation layer is between 0.5 nm and 200 nm.

Ex. 1 ('055 Patent, claim 1) (lettering added).

Independent claim 13 shares a common set of features with claim 1, elements (a)–(h), above. However, claim 13 recites a different wherein clause than that recited in element 1(i), specifically: "wherein the resistance of said Fin active region is reduced by enlarging the width of said Fin active region within the oxidation layer as it approaches the bulk silicon substrate" ("Element 13(i)").

C. The Infringing Products

Samsung's devices, chips, and products incorporating its 14 nm FinFET technologies are collectively referred to as the "Accused Bulk FinFET Device." *See* Ex. 2 (Kuhn Report, at App. B). The processor chips that incorporate the Accused Bulk FinFET Device are fabricated using one of Samsung's 14 nm FinFET technologies (*e.g.*, 14LPE, 14LPP). [redacted]

IV. LEGAL STANDARDS

A. Summary Judgment

Summary judgment is proper when the moving party "shows that there is no genuine dispute as to any material fact and the movant is entitled to a judgment as a matter of law." FED. R. CIV. P. 56(a). A dispute is "genuine" only if there is sufficient evidence for a reasonable fact-finder to find for the non-moving party, and "material" only if it could affect the outcome of the case. *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 248-49 (1986). "If the court does not grant

all the relief requested by the motion, it may enter an order stating any material fact — including an item of damages or other relief — that is not genuinely in dispute and treating the fact as established in the case." FED. R. CIV. P. 56(g).

B. Claim Construction

To determine patent infringement, the court must first construe, as a matter of law, the meaning of the patent claims at issue. *Markman v. Westview Instrm'ts, Inc.*, 52 F.3d 967, 976 (Fed. Cir. 1995), *aff'd*, 517 U.S. 370 (1996). In this case, the Court has construed certain terms of the '055 Patent as follows: (1) "the two top corners . . . are chamfered" means the two top corners are "beveled or rounded;" (2) "trapezoid" means "a shape having two parallel sides;" (3) "said first oxidation layer" means "said first oxide layer;" (4) "said second oxidation layer" means "said second oxide layer;" (5) "the vicinity where the Fin active region and gate meets" means "within the width of the dielectric layer, if any, on the sidewall of the gate, where the Fin active region and gate meet;" (6) "the oxidation layer" means "the second oxide layer;" and (7) "or (and)" means "and/or" in the phrase "the top two corners of said Fin active region are chamfered through an oxidation and etching, or (and) annealing process in a hydrogen atmosphere." Dkt. No. 179.

V. KAIST IP US IS ENTITLED TO SUMMARY JUDGMENT OF INFRINGEMENT

A. The Accused Bulk FinFET Device Infringes Independent Claim 1

1. Samsung Concedes that the Limitations of the Preamble, Elements 1(a), 1(c), 1(f), 1(g), and 1(h) Are Met by the Accused Bulk FinFET Device

[redacted]

[redacted] This Court has held that the "double gate" reference in the preamble is not a limitation. Dkt. No. 179 at 17.

The Accused Bulk FinFET Device includes: 1(a) a bulk silicon substrate; 1(c) a second oxide layer which is formed up to a certain height of the Fin active from the surface of bulk silicon substrate; 1(f) a gate which is formed on said first and second oxide layer; 1(g) a source/drain region which is formed on both sides of the Fin active region except where said gate overlaps with the Fin active region; and 1(h) a contact region and a metal layer which are formed at said source/drain and gate contact region. *See* Ex. 2 (Kuhn Report, ¶¶ 78-82, 91-96, 127-53).

[redacted]

There is no genuine issue of material fact that the Accused Bulk FinFET Device meets elements 1(a), 1(c), 1(f), 1(g), and 1(h).

2. Samsung Has Failed to Raise Any Material Disputes as to the Limitations in Elements 1(b), 1(d), 1(e), and 1(i)

a. Element 1(b) – "a Fin active region which is a wall-shape single crystalline silicon on a surface of the bulk silicon substrate and connected to said bulk silicon substrate"

A "Fin active region" is the silicon structure that protrudes from the underlying bulk silicon substrate. *See, e.g.*, Ex. 1 ('055 Patent 5:36-40, Fig. 3a (element 4)); Ex. 2 (Kuhn Report, ¶¶ 86-88). The '055 Patent teaches that the essence of a FinFET is that there is opposing control on both vertical sides of the fin, where both vertical sides of the fin serve as the main channel regions, and with a depletion region that spans the entire width of the fin (fully-depleted) in the "gate cut" direction. Ex. 1 ('055 Patent 2:1-8); Ex. 2 (Kuhn Report, ¶¶ 84-85).

[redacted]

This is illustrated below.

[redacted]

[redacted]

Despite the evidence to the contrary, Dr. Subramanian argues in his expert report that [redacted]

These arguments are meritless, and fail to raise any genuine disputes as to any material facts.

i. Curved Sidewalls Are Not Excluded from "Wall-Shape"

Dr. Subramanian's first argument in his expert report [redacted] This proposed construction lacks any legal or factual support.

As an initial matter, [redacted]

[redacted]

[redacted]

Moreover, "the specification and prosecution history only compel departure from the plain meaning in two instances: lexicography and disavowal." *GE Lighting Sols., LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014). Here, there is no relevant lexicography or disavowal relating to the term "wall-shape." That term is described broadly in the '055 Patent as explained above, and the '055 Patent never states that "wall-shape" must be limited to a structure having multiple flat sides. The '055 Patent actually teaches the opposite.

For example, the '055 Patent teaches that "the resistance of the Fin active region can be reduced by not fixing the width of the Fin active region 4 but gradually increase[ing] the width within the second oxide layer 10 as it approache[s]" the bulk silicon substrate. Ex. 1 ('055 Patent 5:63-66) (emphasis added). Claim 14 teaches that the Fin active region can be shaped like a trapezoid. Claim 15 teaches that the top two corners of the Fin active region can be chamfered (*i.e.*, rounded). In fact, [redacted] Figures 12d and 13d depict Fin active regions including tapered bottom sections. A person of ordinary skill in the art ("POSA") considering all of these combined

teachings would not conclude that the claimed Fin active region must have multiple flat sides. Ex. 2 (Kuhn Report, ¶¶ 87-89, 283, 330-31).

Finally, [redacted] Thus, the Accused Bulk FinFET Device is "wall-shaped" even under Dr. Subramanian's flawed interpretation of the term "wall-shape."

ii. Samsung's Fin Active Region Is Single Crystalline Silicon

As to Dr. Subramanian's second argument, [redacted] Dr. Subramanian's argument is again flawed.

As an initial matter, [redacted]

First, [redacted] Dependent claims are inherently more limiting than independent claims, and limitations from dependent claims cannot be used to limit the scope of independent claims from which they depend. *Trs. of Columbia Univ. v. Symantec Corp.*, 811 F.3d 1359, 1370 (Fed. Cir. 2016) ("[I]n a situation where dependent claims have no meaningful difference other than an added limitation, the independent claim is not restricted by the added limitation in the

dependent claim."). Claim 1 merely recites that the source/drain region is formed on both sides of the Fin active region except where said gate overlaps with the Fin active region without any reference to the source/drain being formed in the Fin active region. Thus, Dr. Subramanian's initial attempt [redacted] is improper.

Second, Dr. Subramanian does not challenge the fact that Samsung's fins are made of a single crystalline silicon. [redacted] Thus, the Accused Bulk FinFET Device includes a Fin active region which is made of a single crystalline substrate, which is all that is required by claim 1.

Third, [redacted]

[redacted] Thus, the source/drain region is "in" the Fin active region for this reason as well.

Fourth, Dr. Subramanian's attempt to limit the scope of claim 1 is also flawed because it is inconsistent with '055 Patent's teachings. For example, the '055 Patent discloses a preferred embodiment where the selective epitaxial layer is grown on the upper surface of the Fin active region except under the gate. Ex. 1 ('055 Patent 6:64-66, 7:62-64). The '055 Patent also discloses that this selective epitaxial layer can be grown to widen the source/drain region (to reduce parasitic resistance), *id.* 7:65-67, wherein the selective epitaxial layer can be made of polysilicon or silicon-germanium, *id.* 7:1-3. In other words, the '055 Patent teaches that a preferred embodiment of the invention includes a device using selective epitaxial layers as the source/drain, where the epitaxial layers are made of something other than single crystalline silicon.

According to Dr. Subramanian logic, [redacted] However, an interpretation of claim language that excludes a preferred embodiment is rarely, if ever, correct. and would require highly persuasive evidentiary support. *See Liebel-Flarsheim Co. v. Medrad, Inc.,* 358 F.3d 898, 913 (Fed. Cir. 2004). Here, Dr. Subramanian cannot point to *any* evidence, much less any highly persuasive evidence, to establish that the preferred embodiment described above should fall outside the scope of claim 1.

In sum, there is no genuine dispute that the Fin active region in the Accused Bulk FinFET Device is made of a single crystalline silicon.

iii. [redacted] Importing a specific limitation from a dependent claim into an independent claims is improper. *See supra* Section V.A.1.a.ii. And claim 1 lacks any limitations relating to the Fin active region's top two corners. Therefore, this argument must be rejected.

Claim 15 describes the result of a process in which the Fin had two top corners during fabrication, but those corners were then chamfered. [redacted] Claim 1 describes the completed device.

In sum, there is no *genuine* issue of material fact that the Accused Bulk FinFET Device meets claim element 1(b).

b. Element 1(d) – "a gate oxide layer which is formed on both side-walls of the Fin active region protruded from said second oxide layer"

A gate oxide layer can generally be described as a gate dielectric made of oxide, which is positioned between the Fin active region and the gate. *See, e.g.*, Ex. 1 ('055 Patent 5:42-47, Fig. 3a) (illustrating the gate oxide layer as element 12). A gate oxide layer, when surrounded by the gate, and when a potential is applied to the gate, allows for control of the channel regions, potentially in cooperation with additional gate oxide layers. Ex. 2 (Kuhn Report, ¶ 98). In the '055 Patent, the oxide layers on the side-walls of the Fin active region are characterized as the gate oxide layer (as opposed to the first oxide layer, which is located on the upper surface of the fin). Ex. 1 ('055 Patent, 5:42-47); Ex. 2 (Kuhn Report, ¶¶ 97-98).

[redacted]

In particular, as would be understood by a POSA, [redacted]

[redacted]

Dr. Subramanian argues that this limitation is not met because [redacted]

[redacted] This interpretation is untenable.

It is also well-settled that "unless compelled to do otherwise, a court will give a claim term the full range of its ordinary meaning as understood by an artisan or ordinary skill." *Rexnord Corp. v. Laitram Corp.*, 274 F.3d 1336, 1342 (Fed. Cir. 2001). Here, the full range of the terms "gate oxide layer" and "first oxide layer" do not require those layers to be completely separate and distinct from one another.

Further, "the use of two terms in a claim requires that they connote different meanings, not that they refer to two different structures." *Applied Med. Res. Corp. v . U.S. Surgical Corp.*, 448 F.3d 1324, 1333 n.3 (Fed. Cir. 2006). The Federal Circuit has long held that a single structure may satisfy multiple claim elements absent a construction to the contrary. *See Intellectual Prop. Dev., Inc. v. UA-Columbia Cablevision of Westchester, Inc.*, 336 F.3d 1308, 1320 n. 9 (Fed. Cir. 2003) (citing *In re Kelley*, 305 F.2d 909, 915-16 (C.C.P.A. 1962) ("[W]e see no reason why, as a matter of law, one claim limitation may not be responsive to another merely because they are located in the same physical structure.")).

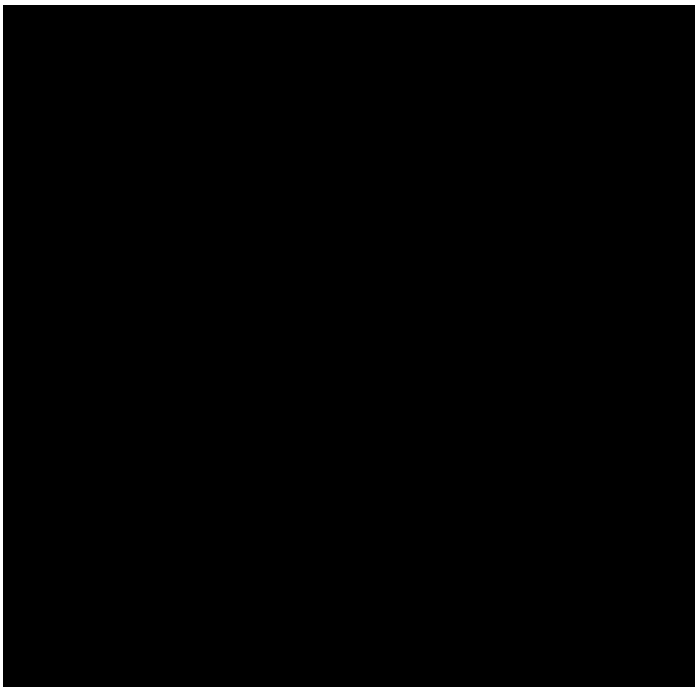
Here, Dr. Subramanian's argument is directly contradicted by a preferred embodiment of the invention. For example, Figs. 3a, 3b, and 4a all illustrate an embodiment of the invention including a gate oxide layer 12 and first oxide layer 6. Ex. 1 ('055 Patent, 4:62-67). As is obvious from those figures, the first and gate oxide layers are not separate and distinct. *See also* Dkt. 179, at 15 ("Layer 12 surrounds the Fin active region on the sides *and on the top*. ['055 Patent] fig.9d.") (emphasis in original); [redacted]

[redacted] Rather, it is one continuous oxide layer that surrounds Fin active region 4, and the first and gate oxide layers are assigned separate names based on its relative location to the Fin active region. The labels and markings used in Fig. 3b make this abundantly clear.

Additionally, no lexicography or disclaimer supports Dr. Subramanian's interpretation. Indeed, even Dr. Subramanian admits [redacted] Thus, Dr. Subramanian's overly restrictive claim interpretation should be rejected. This conclusion is further supported by the fact that Dr. Subramanian's proposed construction would exclude a preferred embodiment (*i.e.*, the Fig. 3a embodiment), which is improper. *Liebel-Flarsheim*, 358 F.3d at 913.

Finally, [redacted]

[2] KAIST IP US will provide the Court with final drafts to replace the rough draft transcript, as well as this image taken of Exhibit 4 from the rough draft transcript, of the deposition of Samsung's expert Dr. Wallace, conducted March 16, 2018 (the day of this filing), as soon as the final transcript is completed.



c. Element 1(e) – "a first oxide layer which is formed on the upper surface of said Fin active region with a thickness greater or equal to that of the gate oxide"

As explained above, the first oxide layer is substantially similar to the gate oxide layer except it is located on the upper surface of the Fin active region. *See, e.g.*, Ex. 1 ('055 Patent 5:42-47, Fig. 3a) (illustrating the gate oxide layer as element 6, which is on all surfaces of the Fin active region). Similar to the gate oxide layer,

[redacted]

Further, [redacted]

[redacted]

[redacted]

[redacted]

[redacted]

[redacted]

[redacted]

Samsung's 30(b)(6) witness also testified that [redacted]

[redacted]

[redacted]

[redacted]

[redacted]

[redacted]

[redacted]

[redacted]

[redacted]

[redacted]

[redacted]

[redacted] Samsung is bound by this testimony, and cannot use an expert to contradict it. *United States ex rel. Gudur v. Deloitte Consulting LLP*, 512 F. Supp. 2d 920, 941-42 (S.D. Tex. 2007), *aff'd*, No. 07-20414, 2008 WL 3244000 (5th Cir. Aug. 7, 2008) ("The Fifth Circuit has long held that a nonmoving party may not manufacture a dispute of fact merely to defeat a motion for summary judgment by offering affidavit testimony that contradicts, without explanation, his or her prior sworn testimony."); *Powell v. Dallas Morning News L.P.*, 776 F. Supp. 2d 240, 246-47 (N.D. Tex. 2011), *aff'd*, 486 F. App'x 469 (5th Cir. 2012) (sustaining objections to expert declarations which directly contradict prior testimony).

Despite the evidence and binding testimony to the contrary, [redacted]. But this defense is merely another improper claim construction argument that must be rejected.

[redacted] "Upper surface" relates to the entire surface on the top of the Fin active region. [redacted]

[redacted]

This concept of an upper surface is disclosed by the '055 Patent. For example, Figures 3 and 4 of the '055 Patent demonstrate that there is not necessarily just a single point that is the "upper surface." The '055 Patent also contemplates that the Fin active region can have its corners chamfered during the fabrication process, Ex. 1 ('055 Patent, 6:4-8), which would not be possible if "upper surface" referred to a single point. Further, no lexicography or disclaimer artificially limits the plain meaning of "upper surface" in the manner proposed by Samsung's experts.

[redacted] Samsung's experts did not analyze the thickness of the "upper surface" of the fin and compare it to the thickness of the "sidewalls." [redacted]

Dr. Kuhn [redacted] She measured the

average thickness across the upper surface of the fin and the sidewalls. [redacted] No other alternative average numbers have been presented by Defendants. [redacted]

There is a separate reason why Samsung's defense fails as a matter of law. Its non-infringement defense on this element is premised on the fact that [redacted]

[redacted]

At bottom, Samsung's experts are attempting to argue [redacted]

[redacted]

But it is well-established that "imperfect practice of an invention does not avoid infringement." *Paper Converting Mach. Co. v. Magna-Graphics Corp.*, 745 F.2d 11, 20 (Fed. Cir. 1984). Thus, Samsung's arguments must be rejected. *See also Broadcom Corp. v. Emulex Corp.*, 732 F.3d 1325, 1333 (Fed. Cir. 2013) ("It is well settled that an accused device that 'sometimes, but not always, embodies a claim[] nonetheless infringes.'") (quoting *Bell Commc'ns Research, Inc. v. Vitalink Commc'ns Corp.*, 55 F.3d 615, 612 (Fed. Cir. 1995)).

There is no genuine issue of material fact that the Accused Bulk FinFET Device meets element 1(d).

d. Element 1(i) – "wherein the thickness of said gate oxide layer is between 0.5 nm and 10 nm, and the thickness of said first oxidation layer is between 0.5 nm and 200 nm"

[redacted]

Nonetheless, [redacted]

But as set forth in the Court's claim construction order, the claimed first

oxidation layer simply refers to the first oxide layer. Dkt. No. 179, at 29 ("From the context of the claim, the 'first oxidation layer' is 'first oxide layer.' This is clear from the claim's references to the 'gate oxide' and the 'first oxide layer,' the relative thicknesses of the two, and then the claim's subsequent recitation of the layer thicknesses. Moreover, the specification repeatedly uses the terms interchangeably."). As also noted by the Court, the specification explicitly references the "oxidation layer" as a layer that "is deposited." *Id.* at 29 ("And though Defendants make much of an 'oxidation layer' being a grown layer formed by oxidation, the specification explicitly references the 'oxidation layer' as a layer that 'is deposited.' ['055 Patent] at 9:31-33.").

Moreover, [redacted]

Accordingly, the Court has already rejected the argument that the first oxide layer must be formed by oxidation, as opposed to, for example, being deposited. *Id.* There is no genuine issue of material fact that the Accused Bulk FinFET Device meets the requirements for claim 1.

B. The Accused Bulk FinFET Device Infringes Independent Claim 13

1. Claim 13's Elements Are Met for the Same Reasons as Claim 1 for All Shared Features

Independent claims 1 and 13 share all of the same features except for the last "wherein"

clause. Accordingly, the Accused Bulk FinFET Device includes the features common to both claims 1 and 13 for all the reasons set forth above. *See supra* Section V.A.

2. Element 13(i) – "wherein the resistance of said Fin active region is reduced by enlarging the width of said Fin active region within the oxidation layer as it approaches the bulk silicon substrate"

[redacted]

Dr. Subramanian's sole argument with respect to this limitation is [redacted] But as explained above, the Court has already rejected this argument, holding that "oxidation layer" simply means the "second oxide layer" where the second oxide layer can be made using, among other things, a deposition process. Dkt. No. 179, at 29; *see also* Ex. 3 (Subramanian Dep. Tr., 192:20-193:7) [redacted] As such, there is no genuine issue of material fact that the Accused Bulk FinFET Device meets the requirements for claim 13.

C. The Accused Bulk FinFET Device Infringes Dependent Claims 11-12

[redacted]

[redacted]

D. The Accused Bulk FinFET Device Infringes Dependent Claims 3-4, 6, and 15

[redacted]

VI. CONCLUSION

For the foregoing reasons, KAIST IP US respectfully submits that it is entitled to summary judgment. If the Court does not see fit to grant the entirety of the relief sought herein, KAIST IP US respectfully requests an order with respect to infringement on each claim element that is not genuinely in dispute as established in the case.

Date: March 16, 2018

Respectfully submitted,

/s/ Andrew Y. Choung

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing document was filed electronically in compliance with Local Rule CV-5(a). As such, this notice was served on all counsel who have consented to electronic service, per L.R. CV-5(a)(3)(A), on March 16, 2018.

/s/ Andrew Y. Choung
Andrew Y. Choung

CERTIFICATE OF AUTHORIZATION TO FILE UNDER SEAL

The undersigned hereby certifies that, under L.R. CV-5(a)(7)(B), the foregoing document is filed under seal pursuant to the Court's Protective Order entered in this matter (Dkt. No. 54).

/s/ Andrew Y. Choung
Andrew Y. Choung